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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,794	11/26/2003	Yu-Chang Jong	252011-1790	9066

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EXAMINER	
DANG, TRUNG Q	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,794	JONG ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/26/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-10, 12-15, 17-20, 22-26, and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Furuhata et al. (US Pat. 6,522,587 B1).

With reference to Figs. 6-13 and the description thereof, the reference teaches every limitation of the claims in that it discloses a method of forming an integrated circuit having gate oxide layers with multiple thicknesses, comprising the steps of:

providing a substrate having a first active region **3000**, a second active region **2000**, and a third active region **1000**;

performing a first oxidation to form a first oxide layer **50aL** on the substrate (Fig. 6);

depositing a blanket high temperature oxide layer (HTO) **50bL** with a first thickness (100–200 Å) overlying the substrate (Fig. 7);

forming a first photoresist layer **R3** on the high temperature oxide layer except over the second active region **2000**;

etching the high temperature oxide layer and the underlying first oxide layer on the second active region using the first photoresist layer as an etch mask to expose the substrate (Fig. 8);

removing the first photoresist layer;

performing a second oxidation to form a second oxide layer **22aL** with a second thickness (30-150 Å) less than the first thickness on the second active region **2000** (Fig. 9);

forming a second photoresist layer **R5** overlying the substrate except over the third active region **1000**;

removing the high temperature oxide layer and the underlying first oxide layer on the third active region to expose the substrate (Fig. 11);

removing the second photoresist layer;

performing a third oxidation to form a third oxide layer **20L** with a third thickness (10 - 100 Å) less than the first thickness on the third active region and on the second oxide layer on the second active region (Fig. 12); and

forming a first gate **34** on the high temperature oxide layer on the first active region, a second gate **32** on the second oxide layer on the second active region, and a third gate **30** on the third thermal oxide layer on the third active region (Fig. 13).

For claim 3, see col. 8, lines 24-28 for the transistor **100** (corresponding to the claimed third device region) that is operated at a first voltage level (1.8- 3.3V (col.4, lines 5-6) is a core device region such as sense amplifier.

For claims 7 and 8, see col.8, lines 29-37 and col. 4, lines 6-12 for transistors **200** and **300**, which correspond to the claimed second and first devices, respectively.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having

ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16, 21, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhata et al. as above in view of Eklund et al. (US 2003/0096466 A1).

Furuhata teaches a method of forming an integrated circuit having gate oxide layers with multiple thicknesses as described above. Haruhata differs from the claims in that while active regions in Furuhata are isolated from one another by field insulation layer **18**, the claims call for device separation by shallow trench isolation (STI). Eklund teaches that device isolation structure may be formed by STI, local oxidation of silicon, or any other suitable method (para. [0013]). It would have been obvious to one of ordinary skill in the art to modify the primary reference by forming the field insulation **18** by employing STI method as suggested by Eklund because the selection of alternate methods recognized in the art to make the same would have been within the level of one skilled in the art, absent a showing of criticality by applicants.

5. Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhata et al. as above.

The reference discloses a method of forming an integrated circuit

having gate oxide layers with multiple thicknesses as described above. The difference between the reference and the claims is the thickness of the HTO layer. However, the determination of thickness for the HTO layer would have been obvious to one of ordinary skill in the art since it is well settle that, absent a showing of criticality by applicants, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

09/27/04